University of Mumbai
Examination 2020 under cluster 2

Program: BE Computer Engineering

Curriculum Scheme: Revised 2012

Examination: Third Year Semester V

Course Code: CPC501 and Course Name: Microprocessor

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	Microprocessor 8086 operates at a frequency of_____
Option A:	3 MHz
Option B:	5 MHz
Option C:	8 MHz
Option D:	10 MHz
Q2.	Microprocessor 8086 has total _____ number of address lines for memory access
Option A:	8
Option B:	16
Option C:	20
Option D:	32
Q3.	In 8086 microprocessor which instructions is an example of direct addressing mode instruction.
Option A:	MOV AX, 1000H
Option B:	MOV AX, [1000]
Option C:	MOV AX, BX
Option D:	MOV AX, [BX]
Q4.	If AL= 22H & BL = 44H, what is value of register after execution of instruction MOV AL, BL.
Option A:	AL = 22H & BL = 22H
Option B:	AL = 22H & BL = 44H
Option C:	AL = 44H & BL = 22H
Option D:	AL = 44H & BL = 44H
Q5.	Total number of registers in microprocessor 8086 are
Option A:	16
Option B:	29
Option C:	14
Option D:	20

Q6.	In 8259 PIC, the register that stores all the interrupt requests in the register_____
Option A:	Interrupt Request Register
Option B:	In-Service Register
Option C:	Priority resolver
Option D:	Interrupt Mask Register
Q7.	8086 does not have an on-chip clock generator thus external clock generator _____is used provide the clock signals
Option A:	8286
Option B:	8284
Option C:	8288
Option D:	8282
Q8.	In 8086, The DMA Controller issues the___ signal to 8086 processor to request for the system bus.
Option A:	INTR
Option B:	TEST
Option C:	HLDA
Option D:	HOLD
Q9.	How many Counters are there in Programmable timer IC 8253?
Option A:	4
Option B:	3
Option C:	8
Option D:	6
Q10.	What is maximum size of a memory segment in 8086?
Option A:	64KB
Option B:	64bytes
Option C:	64MB
Option D:	64GB
Q11.	Instruction Queue of 8086 is _____ byte long.
Option A:	4
Option B:	6
Option C:	8
Option D:	5
Q12.	In Pentium, How many floating point pipeline stages are there?
Option A:	3
Option B:	5
Option C:	7
Option D:	8

Q13.	When the AF flag of 8086 is set 1
Option A:	After addition of 8bit number, if carry is generated
Option B:	If result is out of range
Option C:	After addition of lower 4 bits , if carry is generated
Option D:	If result of operation is zero
Q14.	SPARC has registers file of more the_____registers
Option A:	32
Option B:	64
Option C:	16
Option D:	100
Q15.	What are the data lines connected to Bank 2 of 80386 DX?
Option A:	D23-D16
Option B:	D31-D0
Option C:	D15-D8
Option D:	D15 -D0
Q16.	In 80386DX processor which CR (Control Register) store page fault linear address.
Option A:	CR0
Option B:	CR2
Option C:	CR1
Option D:	CR3
Q17.	In 8086 microprocessor, INTR interrupt may be masked using the which flag
Option A:	Direction Flag
Option B:	Overflow Flag
Option C:	Interrupt Flag
Option D:	Trap Flag
Q18.	What will be content of register BL after executing following set of instructions MOV BL, 34H AND BL,F0H
Option A:	BL = 34H
Option B:	BL = F0H
Option C:	BL = 30H
Option D:	BL = 04H
Q19.	Number of 8-bits ports available in 8255 Programmable peripheral interfaces
Option A:	3
Option B:	4
Option C:	2
Option D:	5

Q20.	In 80386, _____ is the mode of the processor immediately after RESET
Option A:	Virtual Mode
Option B:	Protected Mode
Option C:	Real-Mode
Option D:	SMM mode
Q21.	Among eight debug registers in 80386, DR0-DR7, the registers that are reserved by Intel are
Option A:	DR0, DR1, DR2
Option B:	DR4, DR5
Option C:	DR1, DR4
Option D:	DR5, DR6, DR7
Q22.	In 8255 PPI, BSR mode is where individual bits of _____can be set/reset.
Option A:	Port B
Option B:	Port C
Option C:	Port A
Option D:	Port A & Port B
Q23.	The virtual address space available in 80386 is_____
Option A:	32GB
Option B:	64MB
Option C:	32TB
Option D:	64TB
Q24.	Data cache in Pentium processor is a _____ organized as 2-way set associative with _____lines
Option A:	8KB, 16 bytes
Option B:	8KB, 32 bytes
Option C:	4KB,32 bytes
Option D:	4KB, 16 bytes
Q25.	In Pentium processor, using branch prediction logic if the prediction is wrong for branching instructions in U pipeline there is penalty of _____incurred while _____penalty in case predicted wrong for V pipeline
Option A:	3 cycle, 4 cycle
Option B:	4 cycle, 3cycle
Option C:	3cycle, 3cycle
Option D:	4cycle, 6cycle