University of Mumbai
Examination 2020 under cluster 2 (FrCRCE)

Program: BE Electronics Engineering

Curriculum Scheme: Revised 2012

Examination: Third Year Semester VI

Course Code: EXC 601 and Course Name: Basic VLSI Design

Time: 1 hour Max. Marks: 50

==========

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	Pass transistor can be driven through____ pass transistors
Option A:	One
Option B:	No
Option C:	More
Option D:	Two
Q2.	In CMOS domino logic_____ is used
Option A:	two phase clock
Option B:	three phase clock
Option C:	one phase clock
Option D:	four phase clock
Q3.	As the channel length is reduced in a MOS transistor, depletion region width must be
Option A:	Increased
Option B:	Decreased
Option C:	Must not vary
Option D:	Exponentially increased
Q4.	Half-adders have a major limitation in that they cannot _____
Option A:	Accept a carry bit from a present stage
Option B:	Accept a carry bit from a next stage
Option C:	Accept a carry bit from a previous stage
Option D:	Accept a carry bit from the following stages
Q5.	The difference between half adder and full adder is _____
Option A:	Half adder has two inputs while full adder has four inputs
Option B:	Half adder has one output while full adder has two outputs
Option C:	Half adder has two inputs while full adder has three inputs
Option D:	No difference
Q6.	Built-injunction potential Vb of MOS transistor depends on
Option A:	Vdd

Option B:	Vgs
Option C:	substrate doping level
Option D:	oxide thickness
Q7.	In which of the memories, does the data need to refresh?
Option A:	DRAM
Option B:	Flash memory
Option C:	EPROM
Option D:	SRAM
Q8.	Which memory storage is widely used in PCs and Embedded Systems?
Option A:	Non-volatile SRAM
Option B:	DRAM
Option C:	SRAM
Option D:	RAM
Q9.	Features of switch logic approach
Option A:	occupies less area
Option B:	undesirable threshold voltage
Option C:	low power dissipation
Option D:	Varying area
Q10.	How many AND, OR and EXOR gates are required for the configuration of full adder?
Option A:	1, 2, 2
Option B:	2, 1, 2
Option C:	3, 1, 2
Option D:	4, 0, 1
Q11.	The threshold of an n channel MOSFET can be increased by
Option A:	Increasing the channel doping concentration
Option B:	Reducing the channel doping concentration
Option C:	Reducing the gate oxide thickness.
Option D:	Reducing the channel length
Q12.	In CMOS NAND gate, p transistors are connected in
Option A:	Series
Option B:	parallel
Option C:	cascade
Option D:	random
Q13.	In CMOS domino logic_____ is possible
Option A:	inverting structure
Option B:	non inverting structure
Option C:	inverting and non inverting structure

Option D:	very complex design
Q14.	Fowler-Nordheim tunneling is a
Option A:	Erase Method
Option B:	Programming Method
Option C:	Program Method
Option D:	Scaling Method
Q15.	In inverter during logic 1 to 0 transition, capacitance discharges at
Option A:	pull-up resistance
Option B:	pull- down resistance
Option C:	pull-up and down resistance
Option D:	at gate
Q16.	The spacing of interconnect is scaled by
Option A:	A
Option B:	$1/\alpha$
Option C:	α^2
Option D:	$1/\alpha^2$
Q17.	Latch-up is the generation of
Option A:	low impedance path
Option B:	high impedance path
Option C:	low resistance path
Option D:	high resistance path
Q18.	Channel length of MOS depends on
Option A:	Substrate concentration
Option B:	Vgs
Option C:	Vt
Option D:	Vds
Q19.	In a JFET beyond the pinch off voltage , as the drain voltage increases , the drain current
Option A:	Remains almost constant
Option B:	Decreases
Option C:	Increases
Option D:	May increase or decrease
Q20.	In saturation mode operation, gate to drain capacitance is zero due to _____
Option A:	Gate and drain are interconnected
Option B:	Channel length is reduced
Option C:	Inversion layer doesn't exist
Option D:	Drain is connected to ground

Q21.	When MOSFET is operating in saturation region, the gate to source capacitance is?
Option A:	1/2*Cox*W*L
Option B:	2/3*Cox*W*L
Option C:	Cox*W*L
Option D:	1/3*Cox*W*L
Q22.	Enhancement mode MOSFETs are more commonly used as……..
Option A:	Switches
Option B:	Resistors
Option C:	Buffers
Option D:	Capacitors
Q23.	The p-type substrate in a conventional pn -junction isolated integrated circuit should be connected to:
Option A:	nowhere, i.e. left floating
Option B:	DC ground potential
Option C:	the most positive potential available in the circuit
Option D:	the most negative potential available in the circuit
Q24.	The drain of an n-channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_{TH}) of the MOSFET is 1 V. If the drain current (I_D) is 1 mA for VGS = 2 V, then for V_{GS} = 3 V, ID is
Option A:	2mA
Option B:	3mA
Option C:	9mA
Option D:	4mA
Q25.	Sense amplifier produces full logic swing at
Option A:	internal terminal
Option B:	output terminal
Option C:	Ground
Option D:	voltage